

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

EXPRESS MAIL NO. EL521377309US

Applicant : Arthur Abnous, et al.
Application No. : Not Assigned
Filed : Herewith
Title : ARCHITECTURE FOR VERY HIGH-SPEED
DECISION FEEDBACK SEQUENCE
ESTIMATION
Docket No. : 39498/DWR/B600

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Post Office Box 7068
Pasadena, CA 91109-7068
March 12, 2001

Commissioner:

In the Specification

Please replace the paragraph beginning at page 1, under the title CROSS-REFERENCE
TO RELATED APPLICATIONS with the following rewritten paragraph:

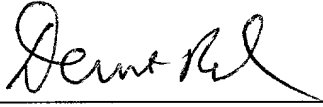
-- The present application claims priority to provisional application Serial Number
60/188,560, filed on March 10, 2000. --

REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By 
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DWR/cah

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

The paragraph beginning at page 1, under the title CROSS-REFERENCE TO RELATED APPLICATIONS has been amended as follows:

The present application claims priority to provisional application Serial Number 60/188,560, filed on March 10, 2000 [is a continuation-in-part of the following patent applications filed on August 09, 1999, commonly owned by the assignee of the present application, the contents of each of which are herein incorporated by reference: Serial Number 09/370,353 entitled "Multi-Pair Transceiver Decoder System with Low Computation Slicer"; Serial Number 09/370,354 entitled "System and Method for High-Speed Decoding and ISI Compensation in a Multi-Pair Transceiver System"; Serial Number 09/370,370 entitled "System and Method for Trellis Decoding in a Multi-Pair Transceiver System"; and Serial Number 09/370,491 entitled "High-Speed Decoder for a Multi-Pair Gigabit Transceiver". The above applications claim priority on the basis of the following provisional applications: Serial Number 60/108,319 entitled "Gigabit Ethernet Transceiver" filed on November 13, 1998; Serial Number 60/116,946 entitled "Multiple Decision Feedback Equalizer" filed on January 20, 1999; and Serial Number 60/130,616 entitled "Multi-Pair Gigabit Ethernet Transceiver" filed on April 22, 1999].

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